SDR IMPLEMENTATION OF QPSK MODEM WITH AWGN

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***Abstract*—**Software Defined Radio, is an important element of wireless (radio) technology in telecommunication industry. SDR is defined as radio in which some or all of the physical layer functions are software defined. The main goal of SDR is to replace as many as possible analog and digital components with programmable devices. SDR may use different source coding, channel coding and modulation schemes. In this paper the SDR modulation and demodulation is done by using QPSK technique. This paper considered additive white Gaussian Noise (AWGN) channel as the channel model. FPGA is chosen as implementation platform due to its suitability for the real time algorithm implementation. The QPSK modem has been studied and simulated using MATLAB and code was written in Verilog HDL and can be implemented on Spartan-3 XC3S50-PQ208 and Spartan-6 XC6SLX45-3CSG324 FPGA processor using Xilinx ISE 14.7.

Keywords — SDR, QPSK, AWGN, matlab, Verilog. Modelsim, Spartan -3 and Spartan -6

I. INTRODUCTION

Software defined radio[17] is one of the important technologies for the modem wireless or for the radio communication systems. SDRs are flexible, reconfigurable and multi-standard system and capable of providing efficient communication. The implementation of SDR has high level of complexity [1][4] size and performance requirements. For the implementation of SDR design include the high demands and challenges include the implementation of the of complex waveforms.

Modulation is an important component in implementation of SDR. It is a way to improve the tradeoff between spectral efficiency and bit error rate .In modulation the characteristics of carrier signal is changed according to the original baseband signal which contains the data or information. Modulation is a process used to transfer the data through the channel .Digital modulation has advantages over the analog modulation in terms of complexity and cost. PSK is a type of digital modulation. The basic concept of PSK modulation is the phase changes according to the baseband information keeping frequency and amplitude constant. QPSK [2] is a form of PSK, is used in modulation, it can be used to increase the data rate.

The QPSK modem [5] [6] is used to implement the SDR, i.e for both modulation and demodulation process. QPSK modulator consists of two binary PSK [BPSK], the QPSK is preferred because of high data rate i.e the data transmission rate in QPSK is twice than that of BPSK. The Bit Error Rate (BER) over Signal-to-Noise ratio (SNR) for both the modulation schemes is same[1]. To produce the QPSK signal two signals of BPSK are added. In QPSK two bit information is transmitted per interval, the symbol period for QPSK is twice the bit period T=2Tb period [1]. For the transmition of the QPSK signal, it requires half the BW of the corresponding BPSK signal which has an advantage of low throughput consumption with complexity in hardware implementation.

Organization of the paper is as follows. In section II the QPSK modulation and demodulation is discussed. Section III gives the concept of existing method and Section IV briefs about the proposed QPSK modem without noise and with AWGN noise. In Section V the simulation using ModelSim simulator and results are discussed and section VI gives the conclusion.

II. QPSK MODULATION AND DEMODULATION

A. QPSK Modulation

The QPSK modulation implementation consists of two BPSK modulators[9]. QPSK consists of two signals they are in-phase and quadrature phase signals. The in-phase component is multiplied with cose carrier signal and quadrature-phase component is multiplied with sine carrier signal.

Generally there are two types of phase changes. $\pi/4,3\pi/4,5\pi/4,7\pi/4$ and $0, \pi/2, \pi, 3\pi/2$.

TABLE 1. QPSK phase with different states

Input	QPSK Phase

00	0°
01	90°
10	180°
11	270°

The above table shows the phase shifts for four different combinations of data they are 00, 01, 10 and 11, where the first bit represents the in-phase and other represents quadrature phase.

The equation for QPSK is given by

$$s(t) = s_I(t)\cos[2\pi f_c t] - s_Q(t)\sin[2\pi f_c t] \qquad (1)$$

Where Si(t) is the in- phase and Sq(t) is the quadrature- phase components of the modulated signal *s(t)* and they are given by In QPSK modulator in order to generate QPSK carrier signal as n we just need to give the input bit stream of data at the input of the QPSK modulator. These input bits are then divided into odd and even sequences by using the serial to parallel converter. Then the signal will be combined with cosine and sine signal and ultimately we will get the QPSK carrier signal by combining both these signals. By adding both the even and odd signals we can get the QPSK modulated wave.
The in-phase and quadrature-phase equations are given by

$$s_I(t)=\sqrt{\frac{2E}{T}}\cos(2\pi f_c t)\ 0 \le t \le T \qquad (2)$$

$$s_Q(t)=\sqrt{\frac{2E}{T}}\sin(2\pi f_c t)\ 0 \le t \le T \qquad (3)$$

B. *QPSK Demodulation*

Demodulation is a reverse process of modulation in which the original information or data is extracted from the modulated signal [22]. In demodulation part the output of each mixer contains both baseband components and high frequency carrier components. Low pass filtering is required to eliminate the high frequency carrier components. In this paper moving window & dump LPF is used.

C. *AWGN channel*

After modulation the data is sent through the channel. During transmission the data is affected by different type of noise. Here Additive White Gaussian Noise channel model was considered. Because by using AWGN channel it is very easy to imitate the effect of random noises that were added by nature.

III. EXISTING METHOD

In this paper the concepts of existing method which was given in the reference paper 1 was considered. It consists of two proposed methods. In first method QPSK modem is implemented by using the concept of booth multiplier. In Second method ROM concept was introduced to store the values of QPSK phases. In these methods the channel noise was not considered. Here the concept of AWGN channel model was introduced. Both QPSK without AWGN and with AWGN are explained and compared in later sections.

IV. PROPOSED METHODOLOGY

The QPSK modem was discussed and implemented in two ways. In first case the channel noise was not considered where as in second case the AWGN channel noise was considered.

A. *QPSK without AWGN*

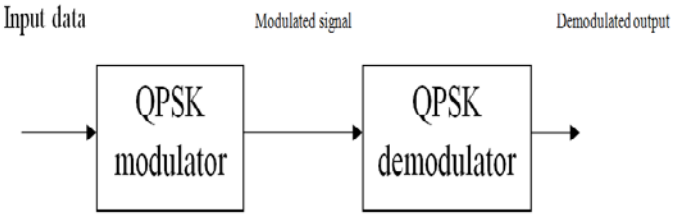

Fig.1 QPSK modem without AWGN

The above figure shows the QPSK modem without noise. In this the QPSK modulated output is transmitted without noise.

B. *QPSK with AWGN*

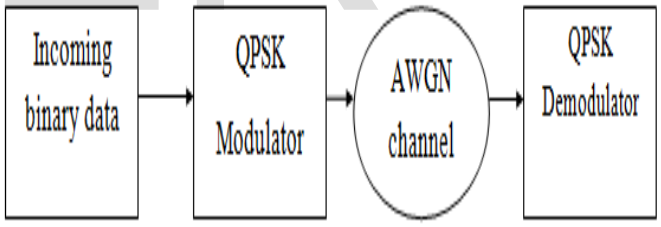

Fig.2 QPSK with AWGN

The block diagram of QPSK modem is as shown in the figure 2. The QPSK modulator modulates the input data and these data is sent through AWGN channel.

C. QPSK transmitter and receiver

i. QPSK transmitter

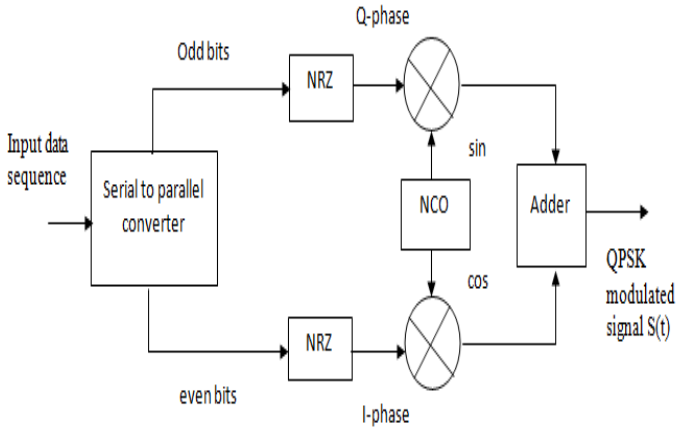

Fig.3 QPSK transmitter

The block diagram QPSK modulator is as shown in the above diagram. It consists of two binary phase shift keying (BPSK) modulators, the serial to parallel converter, which converts data from serial to parallel, and NCO used as carrier generator. The binary serial bit sequence applied to the modulator is converted into two bit parallel sequence of In-phase bit and Quadrature –bit. These I-phase and Q-phase bits are applied to two BPSK modulators whose carrier frequency is orthogonal to each other, which is generated by the NCO carrier generator. The outputs from both the modulators are then added together to get QPSK modulated signal. After modulation the modulated QPSK signal is transmitted through the channel. In this paper we are considering with and without AWGN.

ii. *AWGN*

The AWGN generator was required to generate noise. The characteristics of AWGN channel was discussed in section II. Normally box muller method used to generate AWGN. Here first, we have generated uniformly distributed random noise using LFSR. We know that addition of uniformly distributed random noise gives Gaussian distribution noise. Here four LFSRs are considered to generate uniformly distributed random variables and each LFSR are added to generate Gaussian distribution random noise.

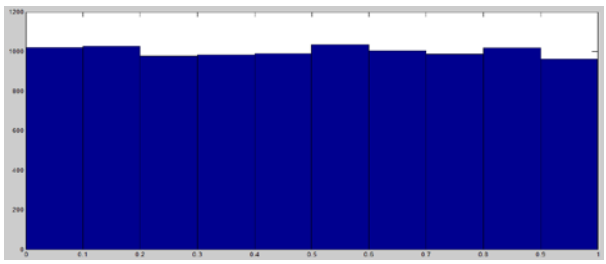

Fig. 4 Histogram of uniform distribution

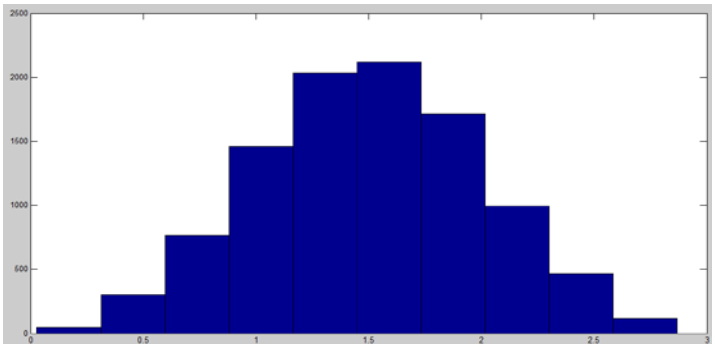

Fig.5 Histogram of Gaussian distribution (addition of uniform distribution)

Fig.6 shows the block diagram of AWGN generator. To generate AWGN we require primitive polynomial expression, ($x^{\circ}+x^{3}$) used as primitive polynomial. Four uniform generators are used to generate uniform distribution function. After that all the results are added together to get Gaussian distribution which gives the AWGN output.

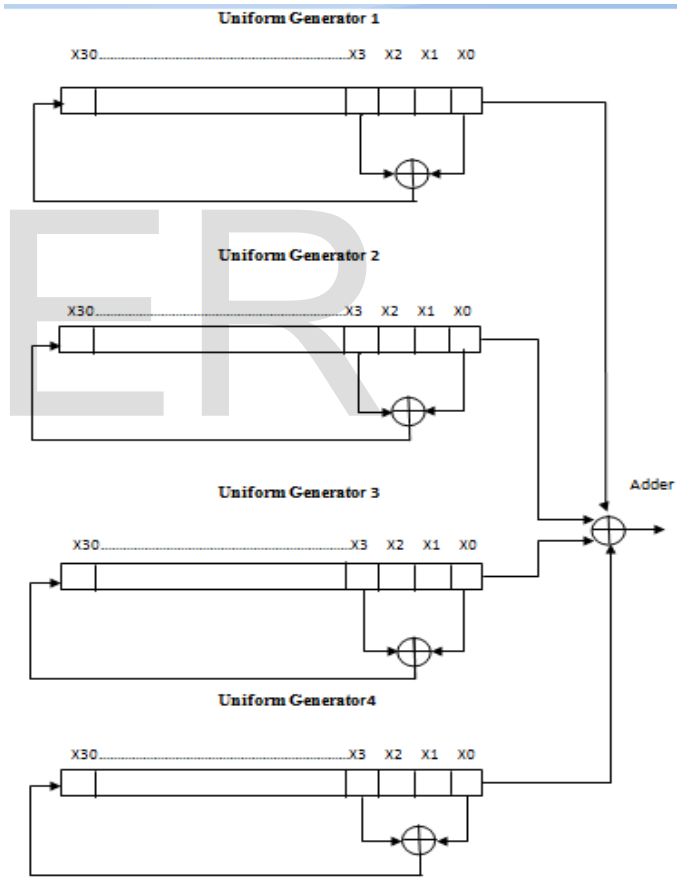

Fig.6 Block diagram of AWGN generator

iii. *QPSK receiver:*

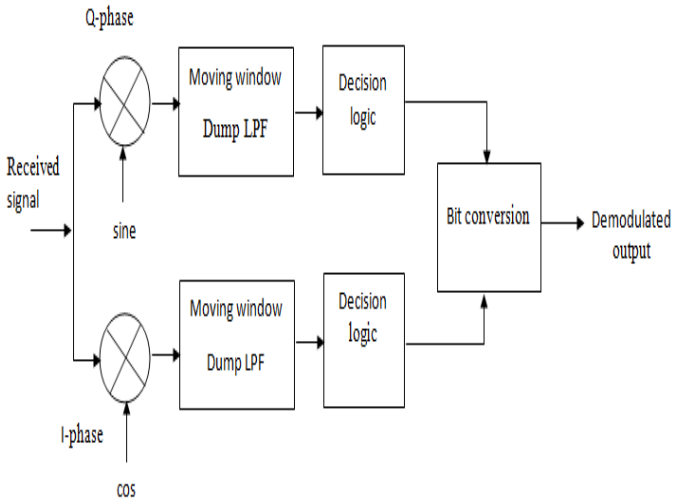

Fig.7 QPSK receiver

The coherent detection method of QPSK demodulation was considered for the demodulation process. The QPSK the signal is applied into the two mixers and they are multiplied with the identical carrier frequency as used in the QPSK modulator. The output of each mixer contains both baseband components which consist of the information message and noise in the form of high frequency components. The low pass filter removes the high frequency components. The moving window & dump filter is used as LPF.

The moving window & dump filter is a special case of FIR filter and it accumulates the samples based on the integration period.

The bit conversion circuit block converts the parallel data to serial. The output of this block gives the demodulated QPSK output.

Table 2: Encoding logic

Incoming data	Encoding bits
00	(1,0)
01	(0,1)
10	(-1,0)
11	(0,-1)

V. SIMULATION AND RESULTS

QPSK modem was first simulated by using matlab. The waveforms are as shown in fig 8 and results are verified.

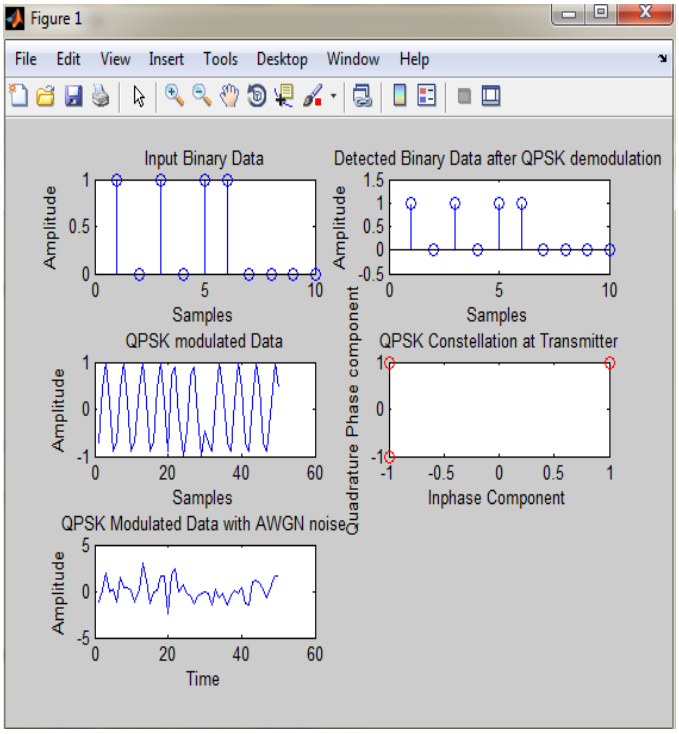

Fig 8. QPSK modem waveform

In this the input binary data is modulated by using QPSK .For different combinations of of input the phase is changed as we discussed in the above sections.The transmitted datal is succesfully retreived by using QPSK demodulator.In this part of matlab code AWGN channel model is considered during communication.

After matlab simulation the code was written in Verilog HDL for both QPSK modem without and QPSK with AWGN.

Xilinx 14.7 ISE version is used for synthesis and simulation. To see the waveforms in anolog format ModelSim simulator is used, the waveforms are given below.

Fig.9 shows the RTL diagram of QPSK modem without AWGN. Fig.11 shows the waveform of QPSK modem without AWGN.

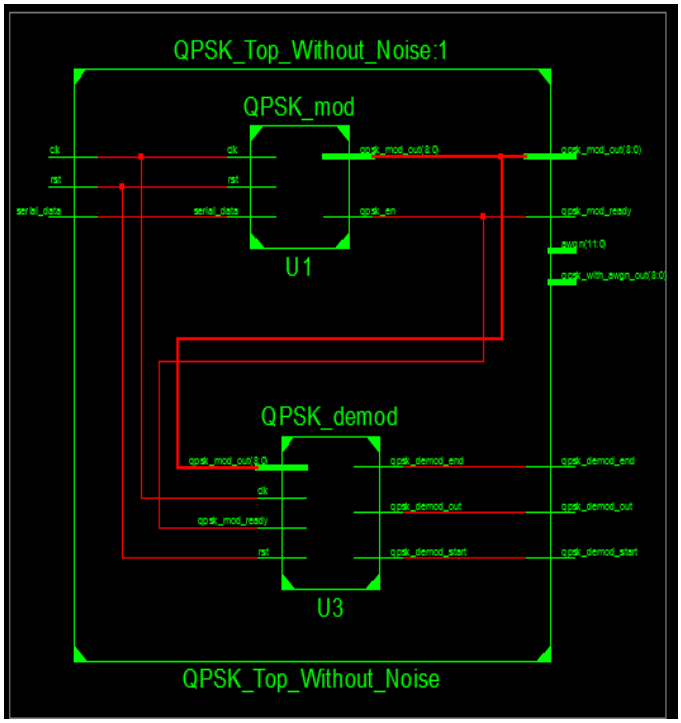

Fig. 9 RTL diagram of QPSK modem

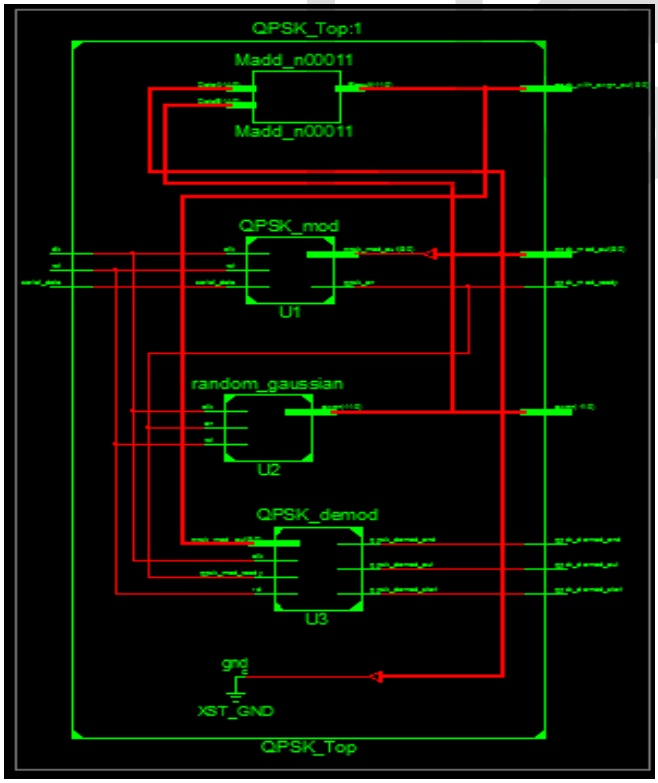

Fig.10 RTL diagram of QPSK modem withAWGN

Fig.10 shows the RTL diagram of QPSK modem with AWGN. In this the AWGN is generated by using LFSR and fig shows the simulation result.

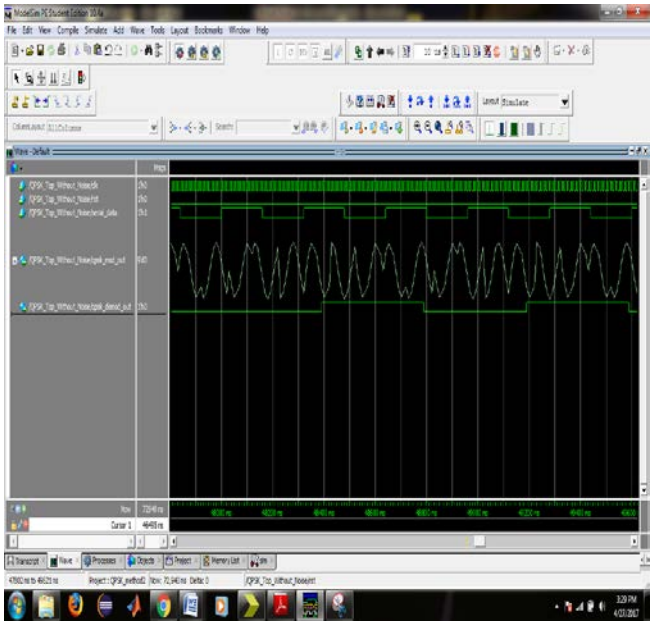

Fig.11 Simulation result of QPSK modem without noise

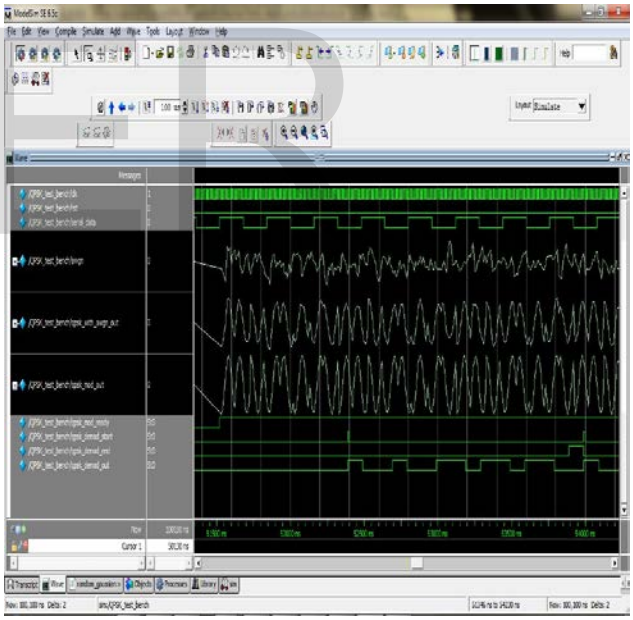

Fig.12 Simulation result of QPSK modem with AWGN

TABLE I. QPSK MODEM WITHOUT AWGN

Parameters	Total usage	Total available on FPGA	% of usage
No. of slice registers	279	54,576	1
No. of slice LUTs	332	27,288	1
No. of occupied slice	110	6,822	1

TABLE II. QPSK MODEM WITH AWGN

Parameters	Total	Total available	Utilization

	usage	on FPGA	
No. of slice registers	437	54,576	1
No. of slice LUTs	390	27288	1
No. of occupied slice	31	6,822	1

TABLE III. COMPARISION OF TWO CASES

	Parame -ters	QPSK without noise	QPSK with noise
Advanced HDL synthesis report	ROMs	256x8-bit single-port block Read Only RAM : 4	256x8-bit single-port block Read Only RAM : 4 4x3-bit single-port distributed Read Only RAM: 1
	Multipliers	8x2-bit multiplier : 2	
	Multiplexe r	1-bit 16-to-1 multiplexer : 3 1-bit 2-to-1 multiplexer : 35 2-bit 2-to-1 multiplexer : 6 32-bit 2-to-1 multiplexer : 6	1-bit 16-to-1 multiplexer : 3 1-bit 2-to-1 multiplexer : 47 1-bit 3-to-1 multiplexer : 10 2-bit 2-to-1 multiplexer : 6 32-bit 2-to-1 multiplexer : 6
	Adder/Sub -tractor	11-bit adder : 1 32-bit adder : 4 4-bit adder : 1	11-bit adder : 1 12-bit adder : 1 32-bit adder : 4 4-bit adder : 1 9-bit adder : 1
	Counters	32-bit up counter : 5 5-bit up counter : 1	32-bit up counter : 5 5-bit up counter : 1
	Accumula -tors	18-bit up loadable accumulator : 2 32-bit-up accumulator : 4	18-bit up loadable accumulator : 2 32-bit up accumulator : 4
	Registers flipflops	244	390
Final report	Cell usage: BELS	BELS : 1773 GND : 1 LUT1 : 337 INV : 71 LUT2 : 200 LUT3 : 78 LUT4 : 24 LUT5 : 51 LUT6 : 88 MUXCY : 436 MUXF7 : 11 MUXF8 : 3 VCC : 1 XORCY : 472	BELS : 1856 GND : 1 INV : 71 LUT1 : 337 LUT2 : 229 LUT3 : 111 LUT4 : 36 LUT5 : 46 LUT6 : 71 MUXCY: 453 MUXF7: 6 MUXF8: 3 VCC : 1 XORCY: 491
	FlipFlops/ Latches	FDC : 73 FDCE : 368 FDRE : 122 FDSE : 2	FDC : 81 FDCE : 435 FDP : 2 FDPE : 57 FDRE : 122 FDSE : 2 LD : 24
	Clock Buffers	BUFGP : 1	BUFG : 1 BUFGP : 1
	IO Buffers	IBUF : 2 OBUF : 13	IBUF : 2 OBUF : 34
Timing Summary	Speed grade: -3	Minimum period: 6.434ns (Maximum Frequency: 155.430MHz)	Minimum period: 6.658ns(Maximum frequency:150.195 MHz)

VI. CONCLUSION

In this paper, the QPSK modem with AWGN was designed for implementation of SDR successfully. The operation of QPSK modem was tested by using matlab. After writing the Verilog HDL code for QPSK modem the results are verified by using ModelSim simulator. Moving window dump FIR filter is used to remove the high frequency noisy components. By comparing the simulation results, the area and power consumption for QPSK modem with AWGN is more. In future the QPSK modem with AWGN can be implemented by using Chip-scope pro to optimize the performance, area and power.

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